Mask Making Tutorial

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Outline

- What Is a Mask and How Is It Used in Semiconductor Lithography?
- What Are the Main Mask-making Steps?
- Why Is Lithography So Difficult?
- Mask Making Eras
- Printing Features With Low k_1 Lithography
- The Mask Maker's Low k_1 Burden
- The Technology Treadmill
- Why Are Mask Costs Increasing So Significantly?
- Some Mask Making Metrics

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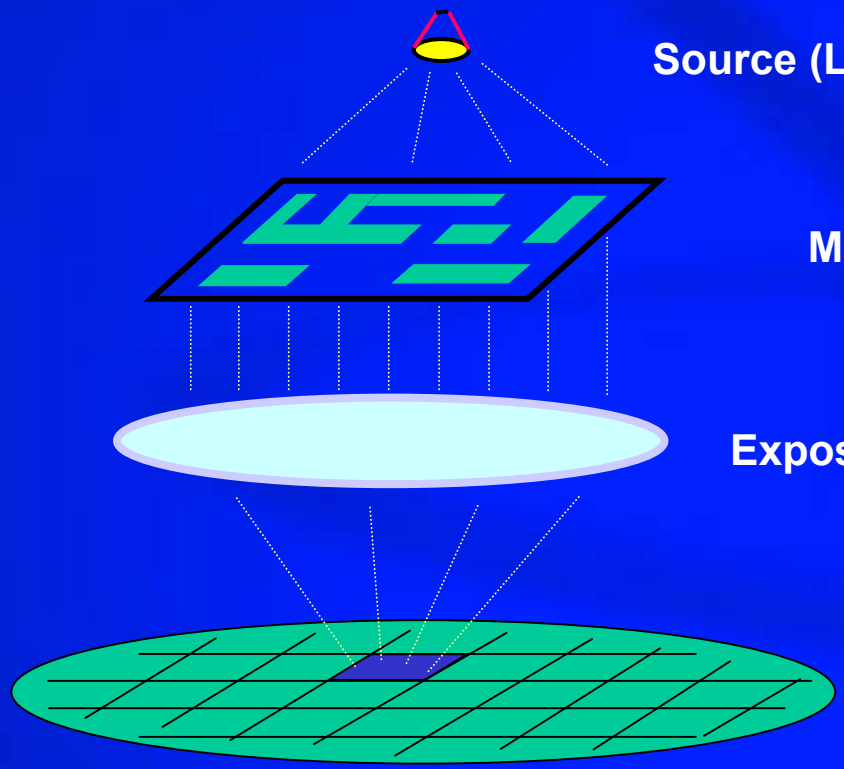
What Is a Mask and How Is It Used in Semiconductor Lithography?



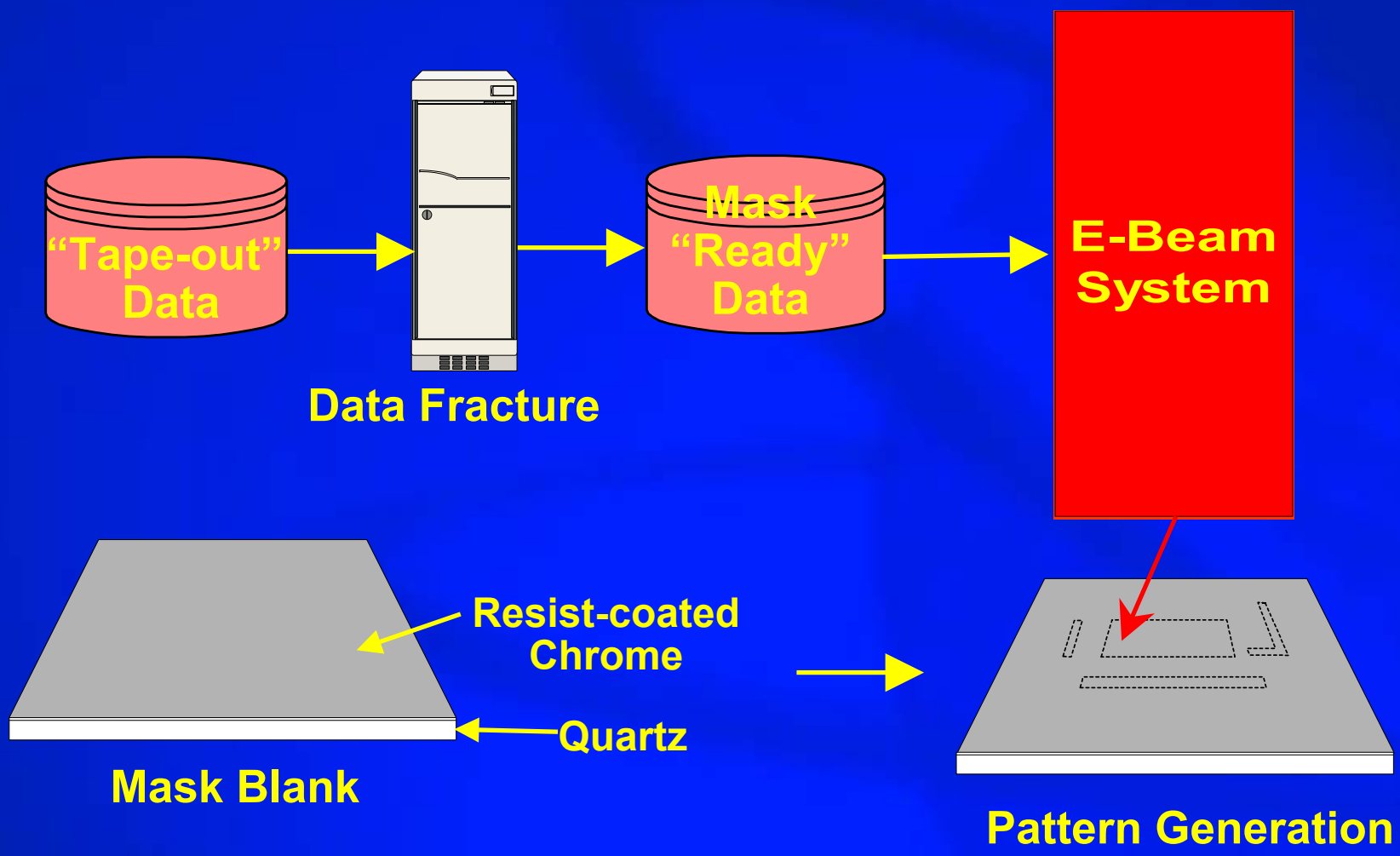
Source (Light bulb)

Mask (Slide)

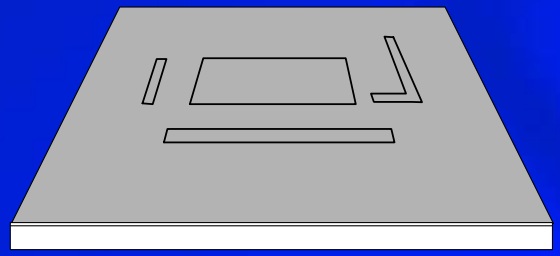
Exposure System (Projector)

Wafer (Screen)

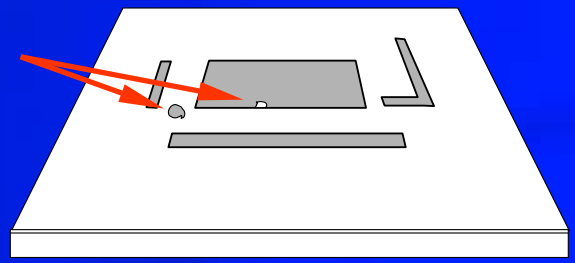
Main Mask-Making Steps



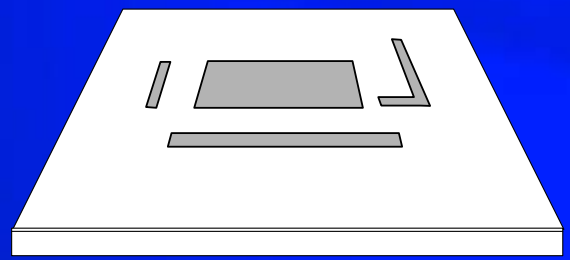
Main Mask-Making Steps



Develop



Etch



Inspect and Repair

Why is Lithography So Difficult?

- Three lithography "knobs" to twist
  - Exposure wavelength (λ)—the smaller the better
  - Lens size (Numerical Aperture—NA)—the larger the better
  - Process complexity factor (k_1)

Feature size = $k_1 \otimes$ wavelength $\div$ lens size

  - » A measure of lithography aggressiveness
  - » Smaller means the ability to print smaller features
- Wavelength scaling has not kept up with the rate of feature size scaling
  - Time and cost to engineer new lasers and exposure systems
- Lens size can only grow so large
  - Size and cost of Lenses; maximum lens size: NA = 1
- Making the process complexity factor smaller has been the area of primary effort

The burden of doing this falls primarily on the mask maker!

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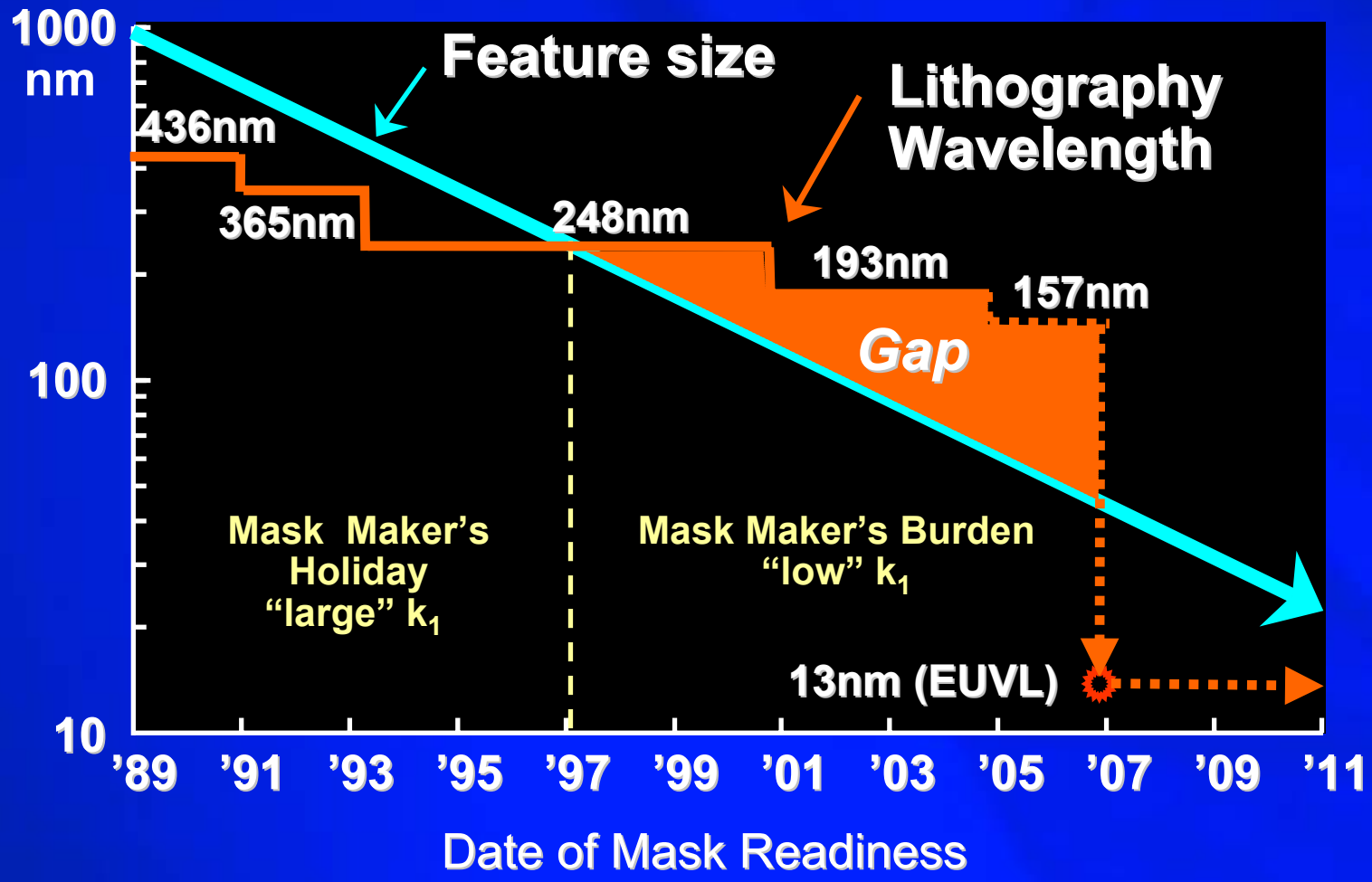
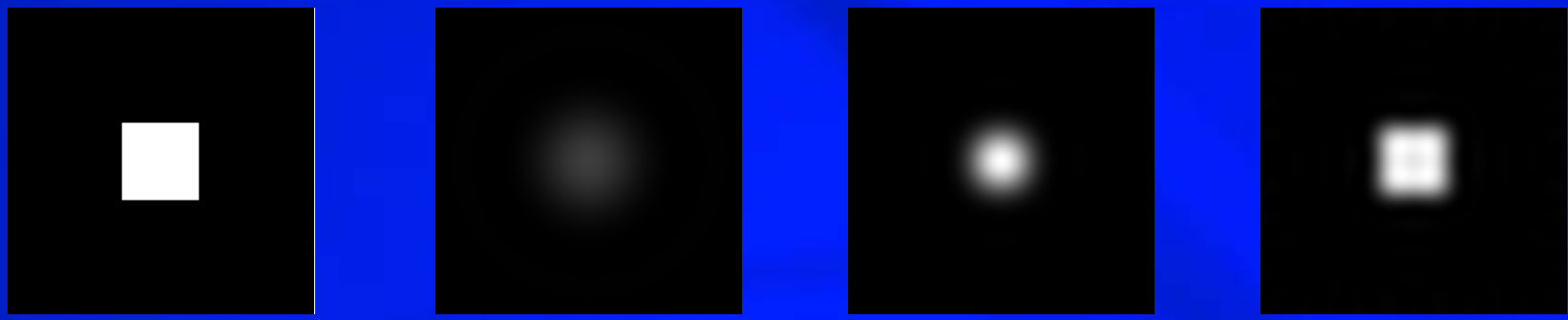
Mask Making Eras



Printing Features With Low k_1 Lithography



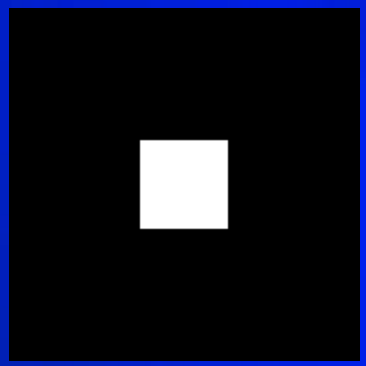
"small" lens "medium" lens "large" lens

What we ask for ⟵ ⟶ What we get

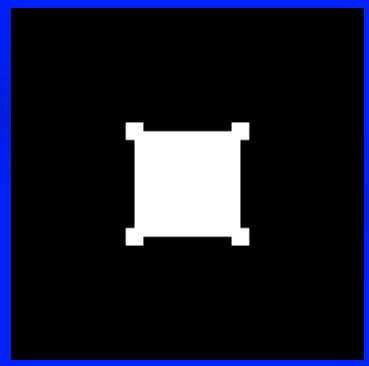
The Mask Maker's Low k_1 Burden

- What we get is not what we asked for
- Solution: Ask for something different
  - This is the idea behind RET (resolution enhancement technology)
- It takes various forms
  - Embellishments (Optical Proximity Correction—OPC features)
  - 3-D structures (Phase-shift Masks)

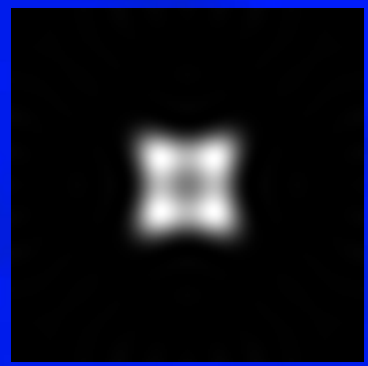
Example of OPC



Want this

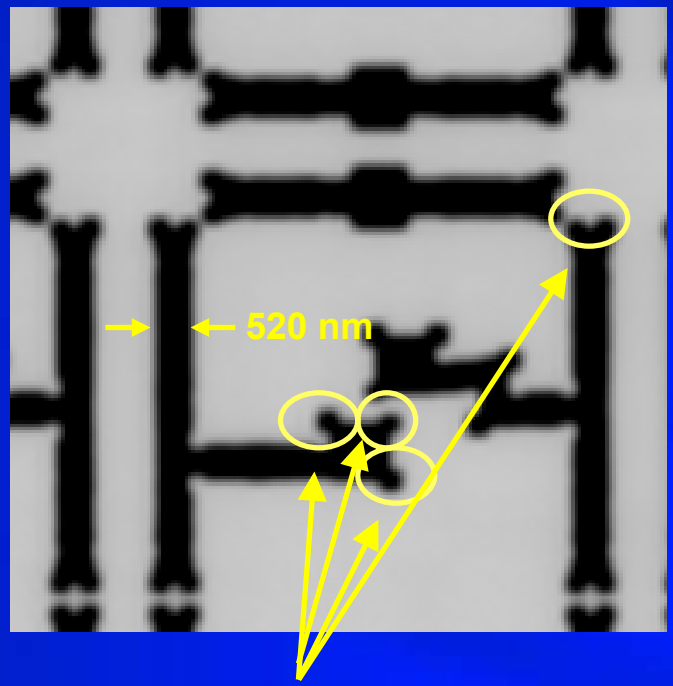


Ask for this
On the mask



Get this
On the wafer

The Mask Maker's Low k_1 Burden—A Real Example



RET "embellishments" must be fully resolved on the mask

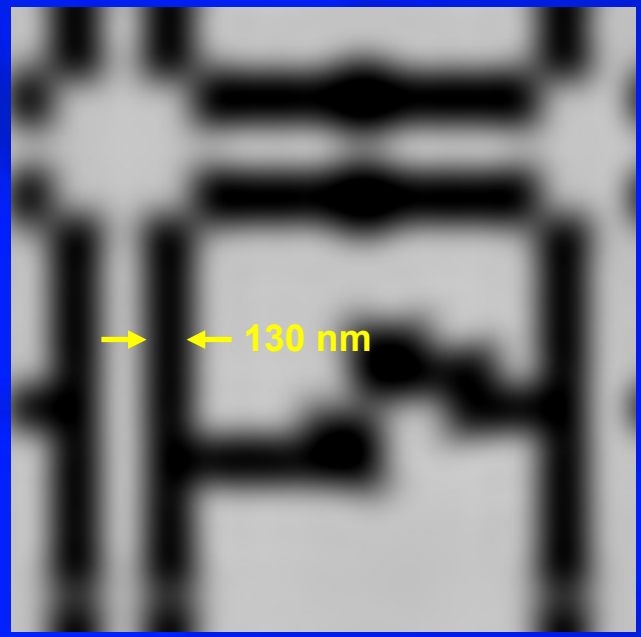
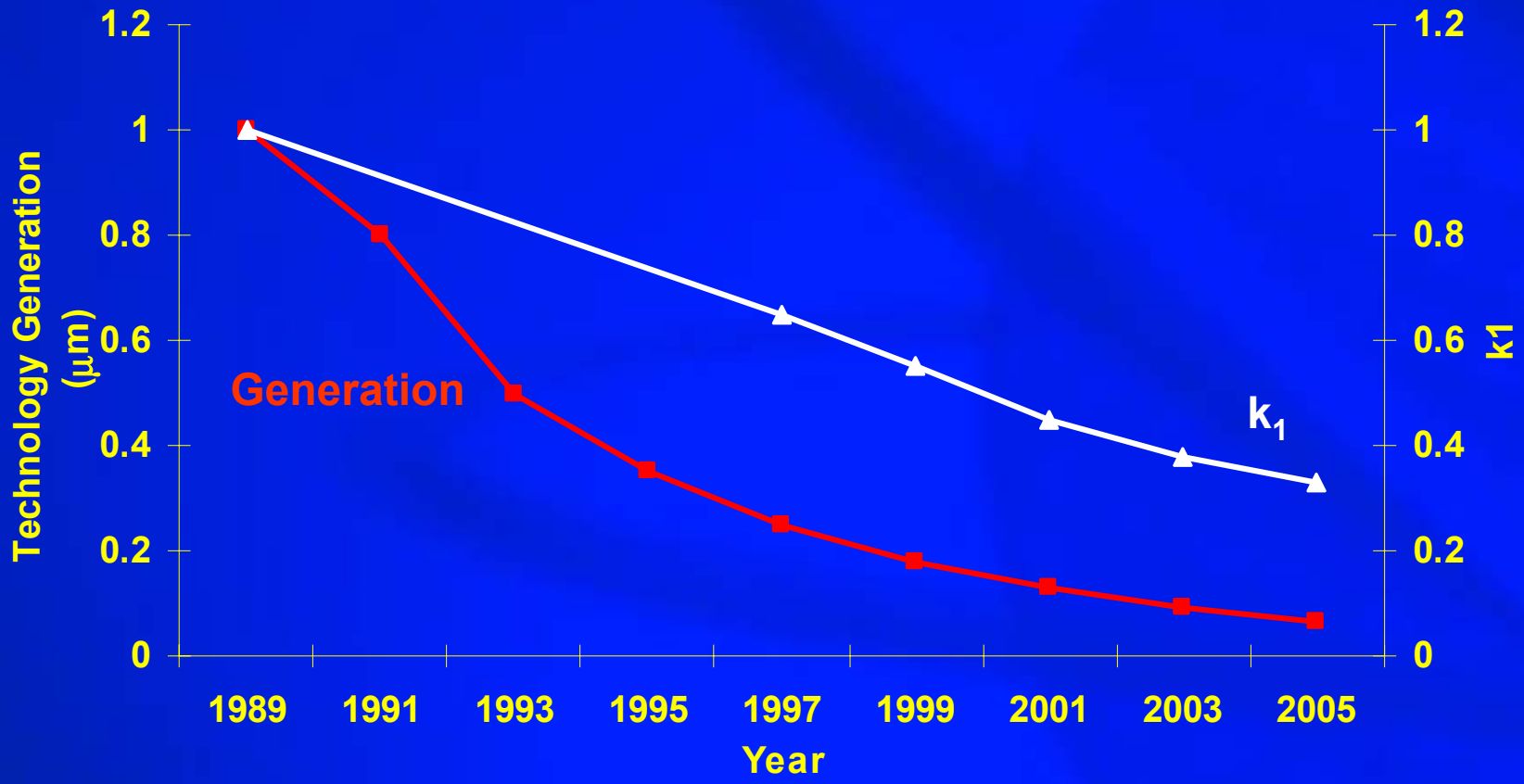


Image on the wafer

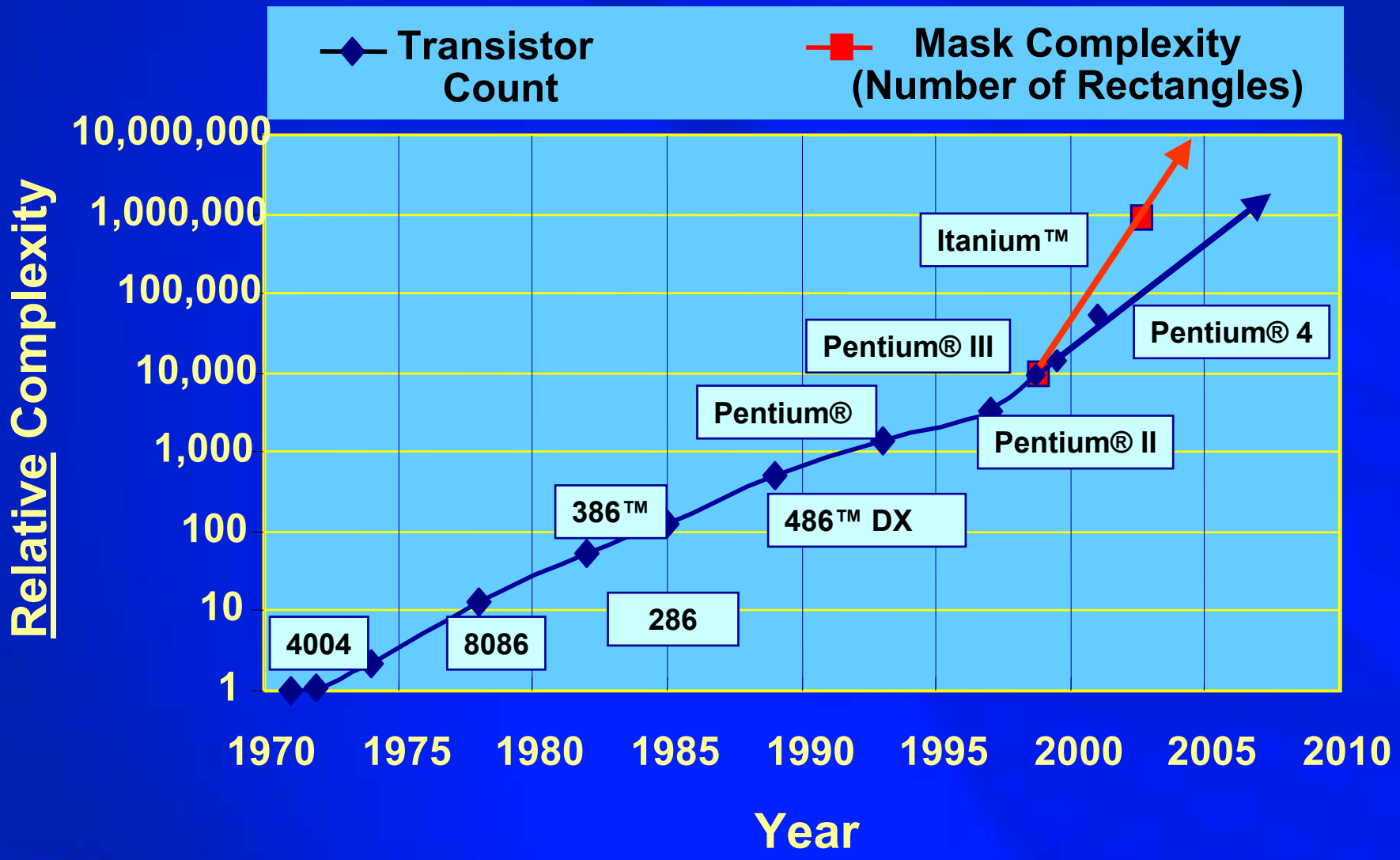
NOT OUT of FOCUS!

The Technology Treadmill

Technology Generation and k_1 Value



Why Are Mask Costs Increasing So Significantly?



Some Mask-Making Metrics and Comparisons

•Pixels:	
–On a 90 nm technology node mask:	1,000,000,000,000
–In a high quality digital photo:	4,000,000
•Defects:	
–Size that must be found and repaired	0.1 micron
–Number of such defects allowed:	0
–Size ratio: defect to the mask area:	size of a basketball / area of California
•Data	
–Typical number of mask layers for 90 nm generation logic product:	22—25
–Total file size needed to specify all these layers:	200 GB
–Time to transmit (design site to mask shop) using T1 line (1.4 MB/sec):	~1.5 days
–Time using T3 line (40 MB/sec):	~1.5 hours
•Cost	
–Cost to lease a T3 line:	$70K/month
–Capital cost to build a 90 nm node capable mask shop (capacity of 200 sets/year @50-70% yield):	$200-250M
–Yearly cost to operate such a shop:	$60-100M
–Cost to make a 90 nm node mask set (depreciation, labor, etc):	~$800K-1.3M